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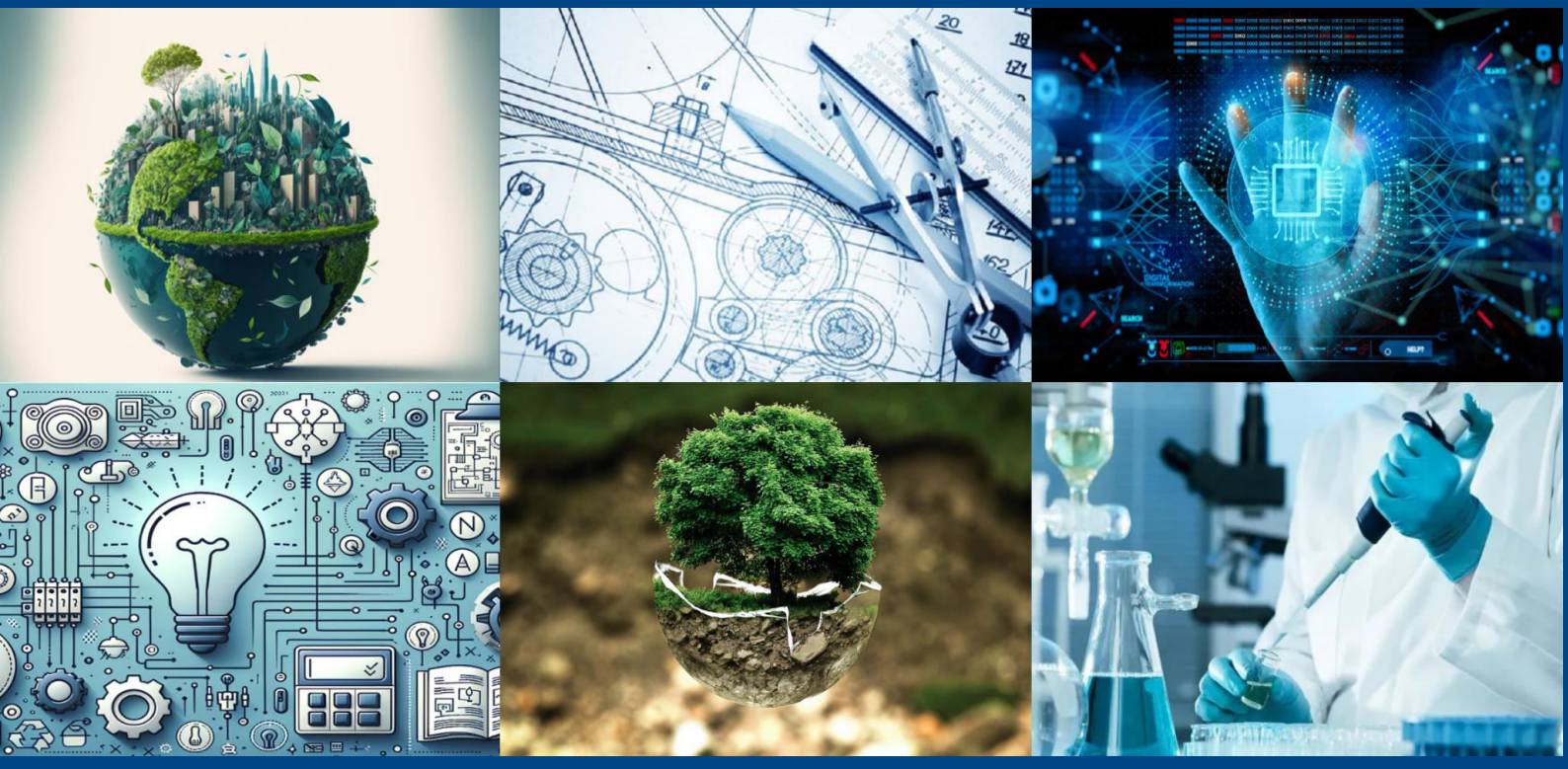

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Design a Three-Stage Comparator Using CMOS Technology

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ABSTRACT: In this paper, a three-stage comparator along with its improved version is proposed to enhance speed and minimize kickback noise. The three-stage comparator in this study has an extra amplification step compared to standard two stage comparator, which enhances the voltage gain and speed. Unlike the standard two stage architecture, which employs PMOS input pairs in the regeneration stage, the three-stage comparator allows NMOS input pairs to be used in both the regeneration and amplification stages, improving efficiency even more. In addition, in the amplification step of the proposed modified three stage comparator, a CMOS input pair is used by cancelling out the NMOS kickback through the PMOS kickback, the kickback noise is considerably reduced. In the regeneration step, it also adds an extra signal line, which helps to boost the speed even more. Both the traditional two stage and the new three stage comparator are built the same 65nm and 45nm CMOS Technology for simple comparisons. The improved version of the three-stage comparator improves speed and reduces kickback noise by 10 times, according to the results. This enhancement come at no expense in terms of input referred offset or noise. Finally, the design was implemented using Tanner EDA, and a comparative analysis was performed for parameters such as area, delay, and power.

KEYWORDS: Kickback Noise, Comparator, High speed.

I. INTRODUCTION

Comparators play a fundamental role in various types of analog-to-digital converters (ADCs), particularly in high-speed and high-resolution designs. The performance of a comparator directly impacts the accuracy, resolution, and sampling rate of the ADC. Therefore, critical design parameters such as speed, offset, input-referred noise, and kickback noise must be carefully optimized. With the increasing demand for ultra-low-power, high-speed, and area-efficient ADCs in modern electronic systems, dynamic regenerative comparators have gained significant attention due to their ability to achieve high performance with low power consumption.

In most ADC architectures, the input signals presented to the comparator are typically small in amplitude. To ensure accurate decision-making, a preamplifier stage is often employed before the comparison stage. This preamplifier generally consists of a differential amplifier with active loads, which provides high gain by amplifying the voltage difference between the two inputs. The output of this stage is then forwarded to the decision-making circuit, commonly implemented using a latch.

A regenerative comparator utilizes latch stages with positive feedback to produce fast and precise decisions. The latch functions as a temporary memory element by storing charge on the gate capacitance of an inverter. Among various latch designs, dynamic latches are widely adopted in analog circuits because they offer excellent speed while maintaining acceptable levels of accuracy. These latches operate in two distinct phases, known as the evaluation phase and the reset phase, both of which are controlled by a clock signal. This phase-based operation enables efficient and timely comparison of input signals, making dynamic regenerative comparators ideal for high-speed, low-power ADC applications.

II. LITERATURE SURVEY

A number of researchers have worked on the proposed topic & here follows a brief review of the works that are carried out by various authors.

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A 1.2-V Dynamic Bias Latch-Type Comparator in 65-nm CMOS With 0.4-mV Input Noise by H. S. Bindra, C. E. Lokin, D. Schinkel, A.-J. Annema, and B. Nauta

A latch-type comparator with a dynamic bias pre-amplifier is implemented in a 65-nm CMOS process. The dynamic bias with a tail capacitor is simple to implement and ensures that the pre-amplifier output nodes are only partially discharged to reduce the energy consumption. The comparator is analyzed and compared to its prior art in terms of energy consumption and input referred noise voltage. First-order equations are presented that show how to optimize the pre-amplifier for low noise and high gain. Both the dynamic bias comparator and the prior art are implemented on the same die and measurements show that the dynamic bias can reduce the average energy consumption by about a factor 2.5 for the same input-equivalent noise at an input common-mode level of half the supply voltage.

A Low-Power High-Speed Comparator for Precise Applications by A. Khorami and M. Sharifkhani

A low-power comparator is presented. PMOS transistors are used at the input of the preamplifier of the comparator as well as the latch stage. Both stages are controlled by a special local clock generator. At the evaluation phase, the latch is activated with a delay to achieve enough preamplification gain and avoid excess power consumption. Meanwhile, small cross-coupled transistors increase the preamplifier gain and decrease the input common mode of the latch to strongly turn on the PMOS transistors (at the latch input) and reduce the delay. Unlike the conventional comparator, the proposed structure let us set the optimum delay for preamplification and avoid excess power consumption. The speed and the power benefits of the comparator were verified using solid analytical derivations, process–VDD–temperature corners, and Monte Carlo simulations along with silicon measurements in 0.18 μm . The tests confirm that the proposed circuit reduces the power consumption by 50% and provides 30% better comparison speed at the same offset and almost the same noise budgets. Moreover, the comparator provides a rail-to-rail input Vcm range in $f$clk=500 MHz.

Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator by S. Babayan-Mashhadi and R. Lotfi

The need for ultra-low-power, area efficient, and high-speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the trade-offs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double-tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18- µm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 2.5 and 1.1 GHz at supply voltages of 1.2 and 0.6 V, while consuming 1.4 mW and 153 µW, respectively. The standard deviation of the input-referred offset is 7.8 mV at 1.2 V supply.

A Low-Power High-Precision Comparator With Time-Domain Bulk-Tuned Offset Cancellation by J. Lu and J. Holleman

A novel time-domain bulk-tuned offset cancellation technique is applied to a low-power high-precision dynamic comparator to reduce its input-referred offset with minimal additional power consumption and delay. The design has been fabricated in a commercially available 0.5-µm process. Measurement results of 10 circuits show a reduction of offset standard deviation from 5.415 mV to 50.57 µV, improved by a factor of 107.1. The offset cancellation scheme does not introduce observable offset or noise, and can achieve fast and robust convergence with a wide range of common mode input. Operating at a supply of 5 V and clock frequency of 200 kHz, the comparator together with the OC circuitry consumes 4.65 µW of power, or 23 pJ of energy per comparison.

III. PROPOSED METHOD

Three-Stage Comparator:

Fig 1 illustrates the three-stage comparator used in this study. The main improvement over Miyahara's comparator is the inclusion of a second-stage preamplifier, which functions as a dynamic inverter. This addition allows the latch stage to use an NMOS input pair, specifically transistors M11 and M12, instead of the traditional PMOS input pair. This modification enhances the speed of the comparator. The preamplifier also contributes to better regeneration efficiency and helps reduce offset and noise.

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However, adding this amplification stage increases the signal propagation time before it reaches the latch. It is necessary to evaluate whether the performance benefits outweigh the additional delay. In the circuit, after the initial amplification, nodes FP and FN are pulled to ground, which creates a full VDD gate-to-source voltage for transistors M8 and M9. These transistors quickly drive the RP and RN nodes high, leading to fast transitions at the output. Simulation results confirm that the second stage reacts faster than the latch stage during post-layout analysis.
This stage operates as a dynamic inverter with low delay, supporting faster response. In comparison to Miyahara's design, the output load on the first stage is smaller, as it only drives M8 and M9, rather than a larger set of transistors. This reduction in loading improves amplification speed.

In conclusion, the proposed comparator architecture includes an additional preamplifier stage between the input and the latch. This preamplifier, implemented using transistors M11 and M12 as an inverter, replaces the PMOS input configuration seen in earlier designs. While the signal must pass through two stages before reaching the latch, this structure provides high voltage gain and reduced noise, with only a minor delay introduced by the added stage.

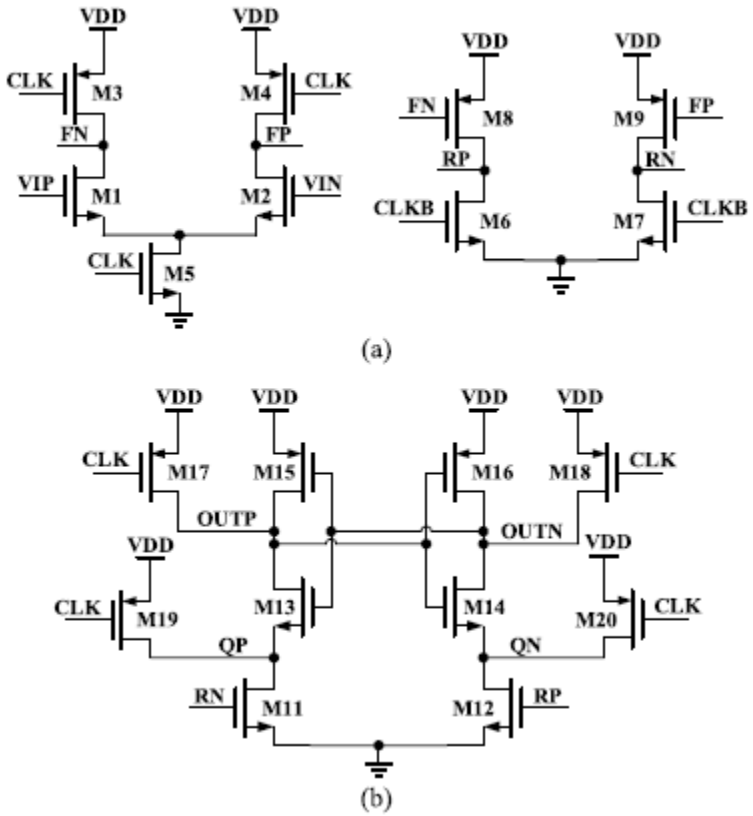

Fig 1: Three-stage comparator in this work. (a) First two stages (preamplifiers). (b) Third stage (latch stage).

Modified Three-Stage Comparator:
To improve the speed of the comparator and reduce kickback noise, a new architecture is introduced using a modified three-stage comparator. As shown in Fig 2, this design is compared to the traditional comparator. The modified model includes a two-stage comparator in Figure 2(b) and a latch stage in Figure 3(c) using transistors M29 to M32. PMOS transistors are used in the first stage of the circuit.

The working of the modified three-stage comparator begins with the reset stage. When the clock (CLK) is at logic 0 and the clock bar (CLKB) is at logic 1, the nodes RP1 and RN1 in Figure 2(b) are connected to ground, and the nodes

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FP1 and FN1 are connected to VDD. In this condition, the transistors M30 and M32 in Figure 2(c) remain off. As a result, no static current flows through transistors M29 to M32 during this time.

In the next stage, which is the amplification stage, CLK goes high (logic 1) and CLKB goes low (logic 0). This causes RP1 and RN1 in Figure 2(c) to rise to VDD, while FP1 and FN1 fall to logic 0. Since RP1 and RN1 rise before FP1 and FN1 fall, this change produces a differential current at the output nodes OUTP and OUTN through the latch stage. This effect comes from an additional signal path shown in Figure 2(c).

The difference in voltage at OUTP and OUTN helps reduce noise and improve the regeneration process. Once FP1 and FN1 fall to logic 0, the extra path in Figure 2(c) is turned off. This improves the overall speed of the comparator and reduces static power consumption

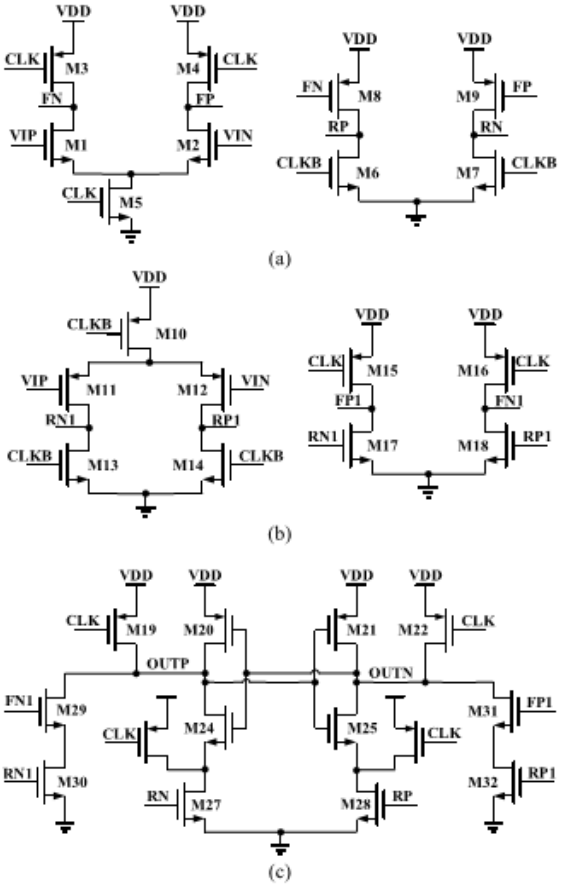

Fig 2: Proposed modified version of three-stage comparator. (a) Original first two stages(preamplifiers) with NMOS input pair. (b) Extra first two stages (preamplifiers)with PMOS input pair. (c) Third stage (latch stage).

Tanner Tool:

The tool used for simulation purpose for the entire research work is Tanner EDA tool version 13.0. The features and functionality of this tool has been described below:

- Schematic Editor (S-Edit): Schematic editor is a powerful design capture and analysis package that can
- generate netlist directly usable in T-Spice simulations.
- T-Spice Circuit Simulator: T-Spice performs fast and accurate simulation of analog and mixed
- analog/digital circuits.
- Waveform Editor (W-Edit): W-Edit is a waveform viewer that provides ease of use, power, and speed

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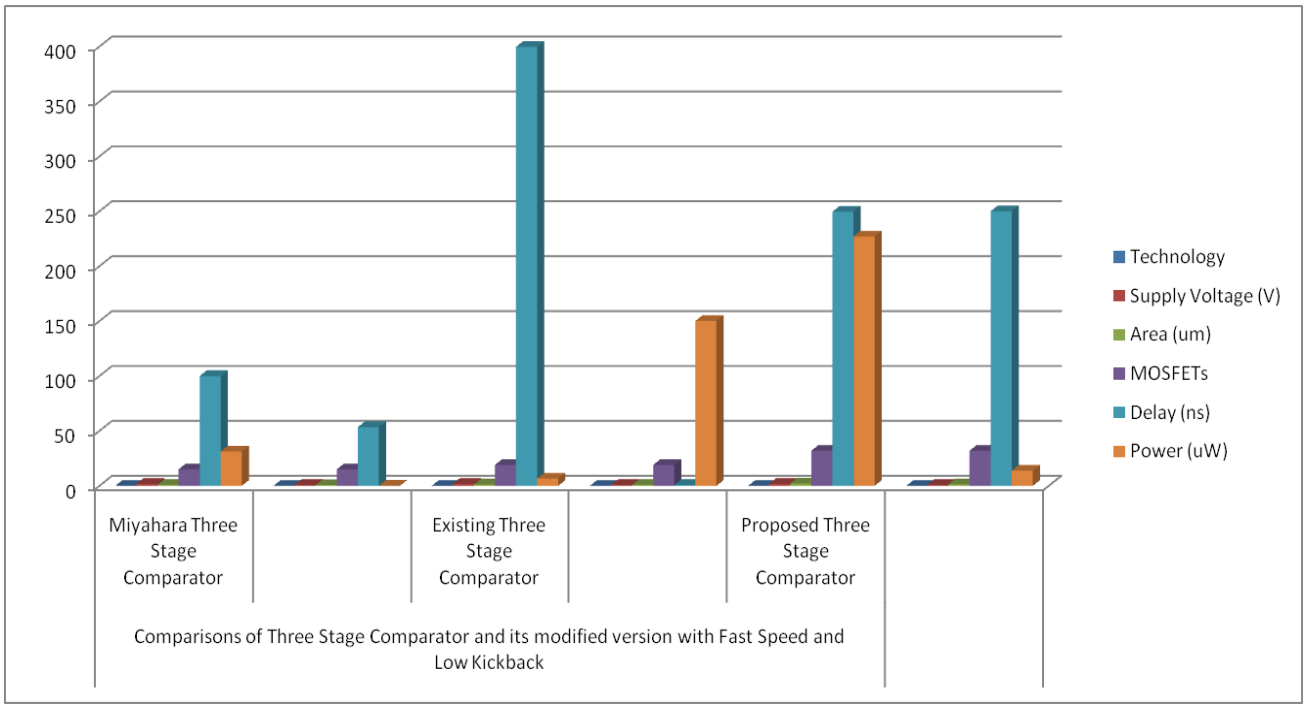
- in a flexible environment designed for graphical data presentation.
- Layout Editor (L-Edit): Tanner EDA tool includes L-Edit for layout editing.

IV. SIMULATED AND MEASURED RESULT

Table 1: Comparision of Three-Stage Comparator and its modified version.

Parameters	Miyahara Two-Stage Comparator		Existing Three-Stage Comparator		Proposed Three-Stage Comparator	
Technology	65nm	45nm	65nm	45nm	65nm	45nm
Supply Voltage	1.8	0.8	1.8	0.8	1.8	0.8
MOSFETs	15	15	19	19	32	32
Delay(ns)	100	53.43	300.49	50.15	250	249.23
Power(uw)	29.723	0.66	35.59	0.854	225.04	13.44

The above table shows that the three-stage comparator and its modified version exhibit the shortest delays, as observed. The modified version also demonstrates minimal kickback noise. Despite the increased circuit complexity, both size and power consumption are reduced. This study presents the three-stage comparator and its improved variant. Both designs operate at high speed, produce minimal kickback noise, and exhibit low input-referred offset and noise. These comparators are particularly suitable for high-speed, high-resolution SAR ADCs. Finally, measurable results confirm the effectiveness and performance of these comparators.



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V. CONCLUSION

This study presents the three-stage comparator and its modified version, both of which demonstrate rapid speed, minimal kickback noise, and low input-referred offset and noise. The modified version, in particular, offers improved performance despite increased circuit complexity, while still maintaining reduced power consumption and area. These comparators are best suited for use in high-speed, high-resolution SAR ADCs. The above table shows that both designs operate efficiently and reliably. Ultimately, quantifiable outcomes confirm how effective and practical these comparators are for modern analog-to-digital conversion systems.

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